Amendments to the Specification:

The below amendments to the specification replaces the corresponding section of the present application:

Please amend Specification, page 7, line 9-page 7, line 20, as follows:

A negative output from summer 106a is provided to a positive input of summer 106b. The output from summer 106a (pd01) is provided to the adjustable delay 102b. The output (pd1) of the phase detector 104b is also provided to the positive input summer 106b. The output (pd1) of summer 106b is provided to adjustable delay 102c. The input of adjustable delay 102c is component clock signal cki2. The output of adjustable delay 102c is provided to the phase detector 104b and phase detector 104c. The phase detector 104c provides an output (pd2) to the negative input of summer 106c. The negative output of summer 106b is provided to the positive input of summer 106c. The input to adjustable delay 102d is component clock signal cki3. The output (pd23) from summer 106 is provided to adjustable delay 102d. The output from adjustable delay 102d is provided to the input of phase detector 104c and the input of phase detector 104d. The output from adjustable delay 102a is also provided to the phase detector 104d.

Please amend Specification, page 8, line 14-page 9, line 2, as follows:

To describe the features of the phase detector and subtractor in more detail refer now to the following description in conjunction with the accompanying

figures. Figure 5 is a diagram for a subtractor and two phase detectors 306a and 306b in accordance with the present invention. Each phase detector 306a and 306b generates a current pulse whose width is proportional to the phase difference between the two input component clock signals, as the current only flows into the branch when both switches 312a, 312b and 314a and 314b ~~atop~~ the current source 308a and 308b are closed at the same time. The subtraction is performed using current summing of the current from the right branch and inverted current from the left branch through a mirror circuit 310. If one phase difference is larger than the other phase difference, voltage on the capacitor 322 will change in a direction to move the common clock edge, e.g., component clock signals ck1, in the two pairs of clock phases, e.g. ck0/ck1 and ckl/ck2, to correct for this difference through the adjustable delay element.